

RCS file: /s6/cvsroot/euterpe/BOM,v

Working file: BOM

head: 5.105

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1940; selected revisions: 33

description:

top level BOM

-----

revision 3.623

date: 1995/04/20 20:53:04; author: tbr; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

2nd try after a problem with a stale entry in my cdio/CVS/Entries file.

Tim

-----

revision 3.622

date: 1995/04/20 20:02:40; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/au

fix place and route so that it converges standalone

-----

revision 3.621

date: 1995/04/20 16:08:56; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/include

Release chages to octlet 6

-----

revision 3.620

date: 1995/04/20 14:52:11; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/tools/el

Release chnges to apd2res

-----

revision 3.619

date: 1995/04/20 05:44:59; author: billz; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/hc

Updated placement to fix NBhc1prbgrant timing path

and cells flopping over clock spar on rhs.

-----

revision 3.618

date: 1995/04/20 04:17:41; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/uu

Minor placement modifications to pack tighter around alignment marks.

-----

revision 3.617

date: 1995/04/19 23:47:09; author: brian1; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/sr

.checkoutrc

sr\_eventreg.pim

Fix nits

-----  
revision 3.616  
date: 1995/04/19 23:44:15; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/nb  
.checkoutrc

Replace clio reference with hard038

-----  
revision 3.615  
date: 1995/04/19 23:42:37; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/hc  
.checkoutrc

Replace clio reference with hard038

-----  
revision 3.614  
date: 1995/04/19 23:40:59; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/dr  
.checkoutrc

Replace clio reference with hard038

-----  
revision 3.613  
date: 1995/04/19 23:39:15; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/ctiod  
.checkoutrc

Replace clio reference with hard038

-----  
revision 3.612  
date: 1995/04/19 04:55:42; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

Pick up all latest cerberus fixes.  
Remove unneeded buft's from top level

-----  
revision 3.611  
date: 1995/04/19 01:28:11; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

cc -- ccseq fix may fix cacchenasty3  
rg -- placement update to avoid collision with au

-----  
revision 3.610  
date: 1995/04/19 00:43:10; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/cc

Fixed not-mutually-exclusive state transition arcs coming  
out of state M1 in ccseq. Thanks to jeffm for sleuthing  
this problem. Updated placement. Looks good.

-----  
revision 3.609  
date: 1995/04/18 19:47:53; author: woody; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

lt, euterpe.V  
Added the logic to support the new Global Access field in cerberus octlet 6.  
Updated placement.

uu:  
Added an additional copy of rDstr2 and vldUW to reduce loading.  
Updated placement. Added in some alignment marks.  
from gards/uu-final:  
    BUT Totals:        3822      27964     59585     45822     38774     18436  
20 paths still fail timing.

passed 5woody.

-----  
revision 3.608  
date: 1995/04/18 17:59:02; author: doi; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/ukernel

rebuild the tests using the recently released ukernel and boot stuff

-----  
revision 3.607  
date: 1995/04/18 17:23:10; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/au

timing fix for extra address bus out duplicated ffs took out buffers

-----  
revision 3.606  
date: 1995/04/18 07:50:54; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

euterpe.status: Add notes on detail bit bugs & cachesize=0 tag X sensitivity.  
icc/iccxc16.Veqn icc/icc.pim.txt: Missing parentheses caused required-PL  
    in ITag of 2 to always cause an exception regardless of current PL.  
    Found by test icache\_except.  
ife/ife.V: Target mispredict sequential new page was treating 8K pg size  
    choice as 4K. Found by inspection. Placement still good.

-----  
revision 3.605  
date: 1995/04/17 22:15:52; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/standalone/uu

Release exrescruel.S

-----  
revision 3.604  
date: 1995/04/17 22:13:36; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/standalone/uu

Take out exresgmshri

-----  
revision 3.603  
date: 1995/04/17 21:45:36; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/standalone/uu

rebuild with realld

-----  
revision 3.602  
date: 1995/04/17 21:35:08; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/standalone/ld

rebuild with realld

-----  
revision 3.601

date: 1995/04/17 19:33:47; author: geert; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/gt

Rebuild gt with new genptab file

Geetr

-----  
revision 3.600

date: 1995/04/17 13:50:05; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/uu

fix genpim to use correct obstruction mask file.

-----  
revision 3.599

date: 1995/04/17 09:31:54; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/cc

cc/at/sr loacation change

-----  
revision 3.598

date: 1995/04/17 09:29:20; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/sr

cc/sr/at location change

-----  
revision 3.597

date: 1995/04/17 09:26:48; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/at

cc/at/sr location change

-----  
revision 3.596

date: 1995/04/16 23:29:25; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/standalone/dp

Rebuild with realld

-----  
revision 3.595

date: 1995/04/16 23:25:27; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify

Makefile.rules

Makefile.defs

Use realld

-----  
revision 3.594

date: 1995/04/16 23:22:59; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/tools

Rebuild with realld

-----  
revision 3.593

date: 1995/04/16 23:03:06; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/tools/el

One cylinder only

-----  
revision 3.592

date: 1995/04/16 03:08:08; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:  
Try a manual placement of ife.V to replace obsolete mincut version. Since  
icc is now much bigger and ife much smaller, ife gets new origin, keeps 20  
atom height, but gives up L shape.  
{icc,ife}/.checkoutrc: fix gards display.

-----  
revision 3.591

date: 1995/04/15 21:14:26; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/au

add components for buffer copy of address output

=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/cerberus.mif,v

Working file: doc/cerberus.mif

head: 4.39

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 53; selected revisions: 1

description:

-----  
revision 4.31

date: 1995/04/19 18:24:07; author: bobm; state: Exp; lines: +8927 -3143  
incorporated review comments and some additional technical corrections.

=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/clock.mif,v

Working file: doc/clock.mif

head: 19.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 6; selected revisions: 1

description:

-----  
revision 19.1

date: 1995/04/19 18:23:35; author: bobm; state: Exp;  
incorporated review comments and some additional technical corrections.

=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/euterpe-microarch.book,v

Working file: doc/euterpe-microarch.book

head: 4.15

branch:

locks: strict

```

access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 1
description:
-----
revision 4.10
date: 1995/04/19 18:26:48;  author: bobm;  state: Exp;  lines: +3 -5
added clock.mif
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/events.mif,v
Working file: doc/events.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
-----
revision 4.18
date: 1995/04/19 18:23:15;  author: bobm;  state: Exp;  lines: +464 -76
incorporated review comments and some additional technical corrections.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/intro.mif,v
Working file: doc/intro.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
-----
revision 4.17
date: 1995/04/19 18:19:20;  author: bobm;  state: Exp;  lines: +1974 -146
incorporated review comments and some additional technical corrections.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/memory.mif,v
Working file: doc/memory.mif
head: 4.36
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
-----
revision 4.28
date: 1995/04/19 18:22:32;  author: bobm;  state: Exp;  lines: +2744 -837
incorporated review comments and some additional technical corrections.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/newchanges.mif,v
Working file: doc/newchanges.mif

```

```

head: 16.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
-----
revision 16.6
date: 1995/04/19 18:25:50; author: bobm; state: Exp; lines: +404 -24
incorporated review comments and some additional technical corrections.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/opcodes.mif,v
Working file: doc/opcodes.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 1
description:
-----
revision 4.19
date: 1995/04/19 18:20:09; author: bobm; state: Exp; lines: +4250 -6350
incorporated review comments and some additional technical corrections.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/pipeline.mif,v
Working file: doc/pipeline.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 27;    selected revisions: 1
description:
-----
revision 4.17
date: 1995/04/19 18:21:54; author: bobm; state: Exp; lines: +1386 -602
incorporated review comments and some additional technical corrections.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/reset.mif,v
Working file: doc/reset.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
-----
revision 4.17
date: 1995/04/19 18:23:26; author: bobm; state: Exp; lines: +275 -31
incorporated review comments and some additional technical corrections.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 11
description:
-----
revision 4.102
date: 1995/04/20 16:08:43;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/include

Release chages to octlet 6
-----
revision 4.101
date: 1995/04/20 14:51:52;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools/el

Release chcnages to apd2res
-----
revision 4.100
date: 1995/04/18 17:58:42;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/ukernel

rebuild the tests using the recently released ukernel and boot stuff
-----
revision 4.99
date: 1995/04/17 22:15:36;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/uu

Release exrescruel.S
-----
revision 4.98
date: 1995/04/17 22:13:18;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/uu

Take out exresgmshri
-----
revision 4.97
date: 1995/04/17 21:45:21;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/uu

rebuild with realld
-----
revision 4.96
date: 1995/04/17 21:34:49;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/ld

rebuild with realld
-----
revision 4.95
date: 1995/04/16 23:29:11;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/dp

```



Rebuild with realld

-----  
revision 4.94

date: 1995/04/16 23:25:13; author: lisar; state: Exp; lines: +3 -3

Release Target: euterpe/verify

Makefile.rules

Makefile.defs

Use realld

-----  
revision 4.93

date: 1995/04/16 23:22:46; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/tools

Rebuild with realld

-----  
revision 4.92

date: 1995/04/16 23:02:52; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/tools/el

One cylinder only

-----  
RCS file: /s6/cvsroot/euterpe/verify/Makefile.defs,v

Working file: verify/Makefile.defs

head: 1.43

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 43; selected revisions: 1

description:

-----  
revision 1.37

date: 1995/04/16 23:24:57; author: lisar; state: Exp; lines: +3 -2

Use realld

-----  
RCS file: /s6/cvsroot/euterpe/verify/Makefile.rules,v

Working file: verify/Makefile.rules

head: 1.72

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 72; selected revisions: 1

description:

-----  
revision 1.63

date: 1995/04/16 23:24:56; author: lisar; state: Exp; lines: +6 -3

Use realld

-----  
RCS file: /s6/cvsroot/euterpe/verify/include/BOM,v

Working file: verify/include/BOM

head: 36.0

branch:

```

locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 27.0
date: 1995/04/20 16:08:34; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/include

Release chages to octlet 6
-----
revision 26.1
date: 1995/04/20 16:08:26; author: lisar; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/include/cerberus.h,v
Working file: verify/include/cerberus.h
head: 10.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 1
description:
-----
revision 10.15
date: 1995/04/19 15:54:31; author: jeffm; state: Exp; lines: +4 -4
Changed mem mgmnt, icache size, and dcache size fields.
=====

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/event/Makefile,v
Working file: verify/obj/processor/event/Makefile
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63;    selected revisions: 2
description:
-----
revision 1.61
date: 1995/04/17 22:11:07; author: lisar; state: Exp; lines: +2 -2
Take out exresgmshri
-----
revision 1.60
date: 1995/04/17 21:42:06; author: lisar; state: Exp; lines: +5 -3
Zero exception count in exlocktest.
Add tests_debug to Makefile.
=====

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:

```

```

locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 1
description:
-----
revision 1.144
date: 1995/04/18 16:56:29; author: lisar; state: Exp; lines: +3 -2
Add pll tests
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/BOM,v
Working file: verify/standalone/BOM
head: 6.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 85;   selected revisions: 5
description:
-----
revision 4.30
date: 1995/04/17 22:15:25; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/standalone/uu

Release exrescruel.S
-----
revision 4.29
date: 1995/04/17 22:13:07; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/standalone/uu

Take out exresgmshri
-----
revision 4.28
date: 1995/04/17 21:45:12; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/standalone/uu

rebuild with realld
-----
revision 4.27
date: 1995/04/17 21:34:39; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/standalone/ld

rebuild with realld
-----
revision 4.26
date: 1995/04/16 23:29:04; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/standalone/dp

Rebuild with realld
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/BOM,v
Working file: verify/standalone/dp/BOM
head: 20.0
branch:
locks: strict

```

```

access list:
keyword substitution: kv
total revisions: 38;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 19.0
date: 1995/04/16 23:28:55; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/standalone/dp

Rebuild with reallld
-----
revision 18.1
date: 1995/04/16 23:28:48; author: lisar; state: Exp; lines: +18 -18
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/Makefile,v
Working file: verify/standalone/dp/Makefile
head: 1.50
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50;    selected revisions: 2
description:
-----
revision 1.50
date: 1995/04/20 14:53:44; author: lisar; state: Exp; lines: +18 -18
Ass rule to make ctd, cti files. By default only make the files
that can be run at the toplevel.
-----
revision 1.49
date: 1995/04/16 23:19:34; author: lisar; state: Exp; lines: +15 -7
Add loop files generation
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/clean-request,v
Working file: verify/standalone/dp/clean-request
head: 1.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 2
description:
-----
revision 1.11
date: 1995/04/20 14:53:42; author: lisar; state: Exp; lines: +2 -0
Ass rule to make ctd, cti files. By default only make the files
that can be run at the toplevel.
-----
revision 1.10
date: 1995/04/16 23:26:46; author: lisar; state: Exp; lines: +1 -0
Rebuild with reallld.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verify/standalone/ld/BOM,v
Working file: verify/standalone/ld/BOM
head: 19.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 38;    selected revisions: 2
description:
-----
revision 17.0
date: 1995/04/17 21:34:29; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/standalone/ld

rebuild with realld
-----

revision 16.1
date: 1995/04/17 21:34:22; author: lisar; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/ld/clean-request,v
Working file: verify/standalone/ld/clean-request
head: 8.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;    selected revisions: 1
description:
-----
revision 8.5
date: 1995/04/17 21:33:54; author: lisar; state: Exp; lines: +1 -0
rebuild with realld
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/NOTES,v
Working file: verify/standalone/nb/NOTES
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
-----
revision 1.14
date: 1995/04/17 20:32:27; author: brian; state: Exp; lines: +16 -30
Added method for causing simultaneous prb requests. Two new addresses
have been added at 0x5000 and 0x6000 for control. See the Notes file.
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/hcperiph.V,v
Working file: verify/standalone/nb/hcperiph.V
head: 2.3
branch:
locks: strict

```

```

access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 2.3
date: 1995/04/17 20:32:29; author: brian; state: Exp; lines: +43 -6
Added method for causing simultaneous prb requests. Two new addresses
have been added at 0x5000 and 0x6000 for control. See the Notes file.
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/nb.h,v
Working file: verify/standalone/nb/nb.h
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 1.2
date: 1995/04/17 20:32:31; author: brian; state: Exp; lines: +3 -1
Added method for causing simultaneous prb requests. Two new addresses
have been added at 0x5000 and 0x6000 for control. See the Notes file.
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/nb_drive.V,v
Working file: verify/standalone/nb/nb_drive.V
head: 1.40
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 40;      selected revisions: 1
description:
-----
revision 1.39
date: 1995/04/17 20:32:32; author: brian; state: Exp; lines: +31 -6
Added method for causing simultaneous prb requests. Two new addresses
have been added at 0x5000 and 0x6000 for control. See the Notes file.
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/nb_drive.h,v
Working file: verify/standalone/nb/nb_drive.h
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 1.2
date: 1995/04/17 20:32:34; author: brian; state: Exp; lines: +8 -1
Added method for causing simultaneous prb requests. Two new addresses
have been added at 0x5000 and 0x6000 for control. See the Notes file.

```

```

=====
RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/periph.V,v
Working file: verify/standalone/nb/periph.V
head: 1.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
-----
revision 1.17
date: 1995/04/17 20:32:36; author: brian; state: Exp; lines: +49 -19
Added method for causing simultaneous prb requests. Two new addresses
have been added at 0x5000 and 0x6000 for control. See the Notes file.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/synctest.vec,v
Working file: verify/standalone/nb/synctest.vec
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;    selected revisions: 2
description:
-----
revision 2.2
date: 1995/04/17 21:21:29; author: brian; state: Exp; lines: +196 -0
added some more cases to the test.
-----
revision 2.1
date: 1995/04/17 20:32:37; author: brian; state: Exp;
Added method for causing simultaneous prb requests. Two new addresses
have been added at 0x5000 and 0x6000 for control. See the Notes file.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/BOM,v
Working file: verify/standalone/uu/BOM
head: 18.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 35;    selected revisions: 6
description:
releasebom adding BOM
-----
revision 16.0
date: 1995/04/17 22:15:12; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/standalone/uu

Release exrescruel.S
-----
revision 15.1
date: 1995/04/17 22:15:03; author: lisar; state: Exp; lines: +2 -2

```

```

releasebom: File needs to be up-to-date to use commit -r
-----
revision 15.0
date: 1995/04/17 22:12:56; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/standalone/uu

Take out exresgmshri
-----
revision 14.1
date: 1995/04/17 22:12:47; author: lisar; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 14.0
date: 1995/04/17 21:45:02; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/standalone/uu

rebuild with realld
-----
revision 13.1
date: 1995/04/17 21:44:55; author: lisar; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Makefile,v
Working file: verify/standalone/uu/Makefile
head: 1.62
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 62; selected revisions: 2
description:
-----
revision 1.61
date: 1995/04/17 22:11:07; author: lisar; state: Exp; lines: +2 -2
Take out exresgmshri
-----
revision 1.60
date: 1995/04/17 21:42:06; author: lisar; state: Exp; lines: +5 -3
Zero exception count in exlocktest.
Add tests_debug to Makefile.
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/clean-request,v
Working file: verify/standalone/uu/clean-request
head: 6.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6; selected revisions: 1
description:
-----
revision 6.5
date: 1995/04/17 21:36:37; author: lisar; state: Exp; lines: +1 -0
rebuild with realld
=====

```



```

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/exlocktest.S,v
Working file: verify/standalone/uu/exlocktest.S
head: 8.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 1
description:
-----
revision 8.4
date: 1995/04/17 21:42:04; author: lisar; state: Exp; lines: +3 -1
Zero exception count in exlocktest.
Add tests_debug to Makefile.
=====

RCS file: /s6/cvsroot/euterpe/verify/tools/BOM,v
Working file: verify/tools/BOM
head: 13.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 90;      selected revisions: 4
description:
releasebom adding BOM
-----
revision 7.1
date: 1995/04/20 14:51:42; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/tools/el

Release chnges to apd2res
-----
revision 7.0
date: 1995/04/16 23:22:37; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/tools

Rebuild with realld
-----
revision 6.2
date: 1995/04/16 23:22:31; author: lisar; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 6.1
date: 1995/04/16 23:02:45; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/tools/el

One cylinder only
=====

RCS file: /s6/cvsroot/euterpe/verify/tools/el/BOM,v
Working file: verify/tools/el/BOM
head: 23.0
branch:
locks: strict
access list:

```

```

keyword substitution: kv
total revisions: 54;    selected revisions: 4
description:
releasebom adding BOM
-----
revision 27.0
date: 1995/04/20 14:51:31;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/tools/el

Release chnges to apd2res
-----
revision 26.1
date: 1995/04/20 14:51:24;  author: lisar;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
-----
revision 26.0
date: 1995/04/16 23:02:36;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/tools/el

One cylinder only
-----
revision 25.1
date: 1995/04/16 23:02:30;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/tools/el/apd2mac1.c,v
Working file: verify/tools/el/apd2mac1.c
head: 1.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;    selected revisions: 1
description:
initial checkin
-----
revision 1.25
date: 1995/04/18 00:35:48;  author: veena;  state: Exp;  lines: +45 -5
Added checks for checking shift overflow and other xlu exception cases. Changed
gcopyswap1swap to gcopyswap11i.
=====

RCS file: /s6/cvsroot/euterpe/verify/tools/el/apd2res1.c,v
Working file: verify/tools/el/apd2res1.c
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63;    selected revisions: 2
description:
initial checkin
-----
revision 1.62
date: 1995/04/18 00:35:52;  author: veena;  state: Exp;  lines: +126 -23
Added checks for checking shift overflow and other xlu exception cases. Changed

```

gcopyswapiswap to gcopyswap11i.

-----  
revision 1.61  
date: 1995/04/16 23:02:01; author: lisar; state: Exp; lines: +7 -1  
only one cylinder does the op, the others b to self.  
Since there is no hold and those tests which take exceptions  
can complete in reasonable time.  
=====

RCS file: /s6/cvsroot/euterpe/verify/tools/el/newchkans.c,v  
Working file: verify/tools/el/newchkans.c  
head: 1.18  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 18; selected revisions: 1  
description:  
-----

revision 1.18  
date: 1995/04/18 00:35:56; author: veena; state: Exp; lines: +2 -2  
Added checks for checking shift overflow and other xlu exception cases. Changed  
gcopyswapiswap to gcopyswap11i.  
=====

RCS file: /s6/cvsroot/euterpe/verify/tools/ld/BOM,v  
Working file: verify/tools/ld/BOM  
head: 24.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 47; selected revisions: 2  
description:  
-----

revision 21.0  
date: 1995/04/16 23:22:14; author: lisar; state: Exp; lines: +1 -1  
Release Target: euterpe/verify/tools

Rebuild with realld  
-----

revision 20.1  
date: 1995/04/16 23:22:08; author: lisar; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r  
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v  
Working file: verify/toplevel/Makefile  
head: 1.185  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 185; selected revisions: 1  
description:  
-----

revision 1.144

date: 1995/04/18 16:56:29; author: lisar; state: Exp; lines: +3 -2  
Add pll tests

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachesynchnasty.S,v  
Working file: verify/toplevel/cachesynchnasty.S

head: 35.5  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 5; selected revisions: 2  
description:

-----  
revision 35.4

date: 1995/04/18 21:01:32; author: jeffm; state: Exp; lines: +13 -1  
Fix to scas result check - thanks again to Lisa Repka.

-----  
revision 35.3

date: 1995/04/17 17:58:11; author: jeffm; state: Exp; lines: +5 -5  
Causing alignment exception - unintentionally. The test was in the  
synch\_check loop, i.e. at the verrrrrry end.

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachesynchnasty2.S,v  
Working file: verify/toplevel/cachesynchnasty2.S

head: 35.10  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 10; selected revisions: 4  
description:

-----  
revision 35.6

date: 1995/04/19 23:11:53; author: jeffm; state: Exp; lines: +29 -37  
Fixed race condition. Passes terp.

-----  
revision 35.5

date: 1995/04/18 21:01:35; author: jeffm; state: Exp; lines: +13 -1  
Fix to scas result check - thanks again to Lisa Repka.

-----  
revision 35.4

date: 1995/04/17 18:00:22; author: jeffm; state: Exp; lines: +5 -5  
Same bug as cachesynchnasty

-----  
revision 35.3

date: 1995/04/17 17:34:10; author: jeffm; state: Exp; lines: +2 -2  
Fix cyl0 hang in rupt handler.

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cnflct\_debug.sig,v  
Working file: verify/toplevel/cnflct\_debug.sig

head: 33.3  
branch:  
locks: strict  
access list:

```

keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 33.2
date: 1995/04/17 20:45:17;  author: jeffm;  state: Exp;  lines: +8 -1
More tracing.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dcacheharder2.S,v
Working file: verify/toplevel/dcacheharder2.S
head: 31.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 1
description:
-----
revision 31.4
date: 1995/04/21 00:59:48;  author: jeffm;  state: Exp;  lines: +5 -38
Updated to use macros in cerberus.h.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/nbhillotest.S,v
Working file: verify/toplevel/nbhillotest.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 35.2
date: 1995/04/19 22:00:29;  author: jeffm;  state: Exp;  lines: +3 -3
Made macros visible to _V version.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/pll.10.10.S,v
Working file: verify/toplevel/pll.10.10.S
head: 35.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 35.1
date: 1995/04/18 16:55:46;  author: lisar;  state: Exp;
Turn on the internal pll
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/pll.S,v
Working file: verify/toplevel/pll.S
head: 35.1

```

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 35.1
date: 1995/04/18 16:55:48;  author: lisar;  state: Exp;
Turn on the internal pll
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/prblm_debug.sig,v
Working file: verify/toplevel/prblm_debug.sig
head: 33.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 2
description:
-----
revision 33.4
date: 1995/04/18 21:24:43;  author: jeffm;  state: Exp;  lines: +1 -3
More tracing - wbck_debug.sig
Removed ltlbmiss from prblm_debug.sig
-----
revision 33.3
date: 1995/04/17 16:54:44;  author: jeffm;  state: Exp;  lines: +18 -0
Added icc debug signals.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/wbck_debug.sig,v
Working file: verify/toplevel/wbck_debug.sig
head: 33.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;     selected revisions: 2
description:
-----
revision 33.4
date: 1995/04/18 21:24:41;  author: jeffm;  state: Exp;  lines: +10 -1
More tracing - wbck_debug.sig
Removed ltlbmiss from prblm_debug.sig
-----
revision 33.3
date: 1995/04/17 22:45:06;  author: jeffm;  state: Exp;  lines: +6 -1
Added cc to nb signals.
=====

RCS file: /s6/cvsroot/euterpe/verify/ukernel/BOM,v
Working file: verify/ukernel/BOM
head: 8.0
branch:
locks: strict

```

...

```

access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 5.0
date: 1995/04/18 17:58:30; author: doi; state: Exp; lines: +1 -1
Release Target: euterpe/verify/ukernel

rebuild the tests using the recently released ukernel and boot stuff
-----
revision 4.1
date: 1995/04/18 17:58:22; author: doi; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/ukernel/Makefile,v
Working file: verify/ukernel/Makefile
head: 1.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
-----
revision 1.7
date: 1995/04/18 17:57:39; author: doi; state: Exp; lines: +8 -12
put the dummy_boot reference back in (I do need it)
=====

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390; selected revisions: 22
description:
top level verilog BOM
-----
revision 3.497
date: 1995/04/20 20:52:48; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

2nd try after a problem with a stale entry in my cdio/CVS/Entries file.

Tim
-----
revision 3.496
date: 1995/04/20 20:02:25; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

fix place and route so that it converges standalone

```

-----  
revision 3.495  
date: 1995/04/20 05:44:45; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/hc

Updated placement to fix NBhc1prbgrant timing path  
and cells flopping over clock spar on rhs.  
-----

revision 3.494  
date: 1995/04/20 04:17:26; author: woody; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/uu

Minor placement modifications to pack tighter around alignment marks.  
-----

revision 3.493  
date: 1995/04/19 23:46:52; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/sr  
    .checkoutrc  
    sr\_eventreg.pim

Fix nits  
-----

revision 3.492  
date: 1995/04/19 23:43:59; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/nb  
    .checkoutrc

Replace clio reference with hard038  
-----

revision 3.491  
date: 1995/04/19 23:42:20; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/hc  
    .checkoutrc

Replace clio reference with hard038  
-----

revision 3.490  
date: 1995/04/19 23:40:44; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/dr  
    .checkoutrc

Replace clio reference with hard038  
-----

revision 3.489  
date: 1995/04/19 23:38:54; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/ctiod  
    .checkoutrc

Replace clio reference with hard038  
-----

revision 3.488  
date: 1995/04/19 04:55:21; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

Pick up all latest cerberus fixes.  
Remove unneeded buft's from top level



```

-----
revision 3.487
date: 1995/04/19 01:27:51; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

cc -- ccseq fix may fix cachenasty3
rg -- placement update to avoid collision with au
-----
revision 3.486
date: 1995/04/19 00:42:40; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

Fixed not-mutually-exclusive state transition arcs coming
out of state M1 in ccseq. Thanks to jeffm for sleuthing
this problem. Updated placement. Looks good.
-----
revision 3.485
date: 1995/04/18 19:47:35; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

lt, euterpe.V
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

uu:
Added an additional copy of rDstr2 and vldUW to reduce loading.
Updated placement. Added in some alignment marks.
from gards/uu-final:
      BJT Totals:      3822      27964      59585      45822      38774      18436
20 paths still fail timing.

passed 5woody.
-----
revision 3.484
date: 1995/04/18 17:22:54; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

timing fix for extra address bus out duplicated ffs took out buffers
-----
revision 3.483
date: 1995/04/18 07:50:38; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

euterpe.status: Add notes on detail bit bugs & cachesize=0 tag X sensitivity.
icc/iccxi6.Vegn icc/icc.pim.txt: Missing parentheses caused required-PL
in ITag of 2 to always cause an exception regardless of current PL.
Found by test icache_except.
ife/ife.V: Target mispredict sequential new page was treating 8K pg size
choice as 4K. Found by inspection. Placement still good.
-----
revision 3.482
date: 1995/04/17 19:33:32; author: geert; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

Rebuild gt with new genptab file

Geetr

```

```

-----
revision 3.481
date: 1995/04/17 13:49:48; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

fix genpim to use correct obstruction mask file.
-----
revision 3.480
date: 1995/04/17 09:31:40; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

cc/at/sr loacation change
-----
revision 3.479
date: 1995/04/17 09:29:06; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

cc/sr/at location change
-----
revision 3.478
date: 1995/04/17 09:26:33; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

cc/at/sr location change
-----
revision 3.477
date: 1995/04/16 03:07:53; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
  Try a manual placement of ife.V to replace obsolete mincut version. Since
  icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
  atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.
-----
revision 3.476
date: 1995/04/15 21:14:08; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

add components for buffer copy of address output
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737; selected revisions: 28
description:
-----
revision 286.0
date: 1995/04/20 20:52:30; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

2nd try after a problem with a stale entry in my cdio/CVS/Entries file.

Tim

```
-----
revision 285.9
date: 1995/04/20 20:52:17; author: tbr; state: Exp; lines: +16 -15
releasebom: File needs to be up-to-date to use commit -r
-----
revision 285.8
date: 1995/04/20 20:02:10; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/au
```

fix place and route so that it converges standalone

```
-----
revision 285.7
date: 1995/04/20 05:44:32; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc
```

Updated placement to fix NBhclprbgrant timing path  
and cells flopping over clock spar on rhs.

```
-----
revision 285.6
date: 1995/04/20 04:17:12; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
```

Minor placement modifications to pack tighter around alignment marks.

```
-----
revision 285.5
date: 1995/04/19 23:46:36; author: brianl; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr
    .checkoutrc
    sr_eventreg.pim
```

Fix nits

```
-----
revision 285.4
date: 1995/04/19 23:43:43; author: brianl; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/nb
    .checkoutrc
```

Replace clio reference with hard038

```
-----
revision 285.3
date: 1995/04/19 23:42:03; author: brianl; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc
    .checkoutrc
```

Replace clio reference with hard038

```
-----
revision 285.2
date: 1995/04/19 23:40:28; author: brianl; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr
    .checkoutrc
```

Replace clio reference with hard038

```
-----
revision 285.1
```

...

date: 1995/04/19 23:38:35; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/ctiod  
.checkoutrc

Replace clio reference with hard038

-----  
revision 285.0  
date: 1995/04/19 04:55:02; author: tbr; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

Pick up all latest cerberus fixes.  
Remove unneeded buft's from top level

-----  
revision 284.1  
date: 1995/04/19 04:54:49; author: tbr; state: Exp; lines: +3 -3  
releasebom: File needs to be up-to-date to use commit -r

-----  
revision 284.0  
date: 1995/04/19 01:27:27; author: billz; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

cc -- ccseq fix may fix cach nasty3  
rg -- placement update to avoid collision with au

-----  
revision 283.2  
date: 1995/04/19 01:27:11; author: billz; state: Exp; lines: +5 -4  
releasebom: File needs to be up-to-date to use commit -r

-----  
revision 283.1  
date: 1995/04/19 00:42:09; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/cc

Fixed not-mutually-exclusive state transition arcs coming  
out of state M1 in ccseq. Thanks to jeffm for sleuthing  
this problem. Updated placement. Looks good.

-----  
revision 283.0  
date: 1995/04/18 19:47:13; author: woody; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

lt, euterpe.V  
Added the logic to support the new Global Access field in cerberus octlet 6.  
Updated placement.

uu:  
Added an additional copy of rDstr2 and vldUW to reduce loading.  
Updated placement. Added in some alignment marks.  
from gards/uu-final:  
BUT Totals: 3822 27964 59585 45822 38774 18436  
20 paths still fail timing.

passed 5woody.

-----  
revision 282.2  
date: 1995/04/18 19:46:56; author: woody; state: Exp; lines: +9 -9  
releasebom: File needs to be up-to-date to use commit -r

```

-----
revision 282.1
date: 1995/04/18 17:22:38; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

timing fix for extra address bus out duplicated ffs took out buffers
-----
revision 282.0
date: 1995/04/18 07:50:19; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.status: Add notes on detail bit bugs & cachesize=0 tag X sensitivity.
icc/iccxc16.Veqn icc/icc.pim.txt: Missing parentheses caused required-PL
    in ITag of 2 to always cause an exception regardless of current FL.
    Found by test icache_except.
ife/ife.V: Target mispredict sequential new page was treating 8K pg size
    choice as 4K. Found by inspection. Placement still good.
-----
revision 281.6
date: 1995/04/18 07:50:05; author: mws; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
-----
revision 281.5
date: 1995/04/17 19:33:18; author: geert; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

Rebuild gt with new genptab file

Geetr
-----
revision 281.4
date: 1995/04/17 13:49:32; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

fix genpim to use correct obstruction mask file.
-----
revision 281.3
date: 1995/04/17 09:31:26; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

cc/at/sr location change
-----
revision 281.2
date: 1995/04/17 09:28:52; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

cc/sr/at location change
-----
revision 281.1
date: 1995/04/17 09:26:19; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

cc/at/sr location change
-----
revision 281.0
date: 1995/04/16 03:07:35; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

```
ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
  Try a manual placement of ife.V to replace obsolete mincut version. Since
  icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
  atom height, but gives up L shape.
[icc,ife]/.checkoutrc: fix gards display.
```

```
-----
revision 280.2
```

```
date: 1995/04/16 03:07:24; author: mws; state: Exp; lines: +4 -4
```

```
releasebom: File needs to be up-to-date to use commit -r
```

```
-----
revision 280.1
```

```
date: 1995/04/15 21:13:48; author: dickson; state: Exp; lines: +2 -2
```

```
Release Target: euterpe/verilog/bsrc/au
```

```
add components for buffer copy of address output
```

```
-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
```

```
Working file: verilog/bsrc/Makefile
```

```
head: 1.255
```

```
branch:
```

```
locks: strict
```

```
access list:
```

```
keyword substitution: kv
```

```
total revisions: 255; selected revisions: 4
```

```
description:
```

```
-----
revision 1.236
```

```
date: 1995/04/20 14:17:17; author: lisar; state: Exp; lines: +17 -9
```

```
Added a rule to compv to make sure the
cg/cgclockbias.v_for_use_with_squelsh_buffer
is used.
```

```
-----
revision 1.235
```

```
date: 1995/04/18 20:44:12; author: tbr; state: Exp; lines: +3 -3
```

```
clean out geert exclude list
```

```
-----
revision 1.234
```

```
date: 1995/04/17 04:55:31; author: tbr; state: Exp; lines: +3 -2
```

```
.PRECIOUS .splvs. Change tbr exclude list
```

```
-----
revision 1.233
```

```
date: 1995/04/15 18:18:14; author: lisar; state: Exp; lines: +2 -2
```

```
Correct typo in simfiles
```

```
-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
```

```
Working file: verilog/bsrc/Makefile.tst
```

```
head: 40.104
```

```
branch:
```

```
locks: strict
```

```
access list:
```

```
keyword substitution: kv
```

```
total revisions: 104; selected revisions: 2
```

```
description:
```

```

revision 40.68
date: 1995/04/17 20:58:51; author: tbr; state: Exp; lines: +3 -3
new dependency for power.tab.top
-----
revision 40.67
date: 1995/04/17 04:53:19; author: tbr; state: Exp; lines: +3 -3
uu .obs filename change
=====

RCS file: /s6/cvsroot/eutерpe/verilog/bsrc/Makefile.vo,v
Working file: verilog/bsrc/Makefile.vo
head: 27.45
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 45; selected revisions: 1
description:
-----
revision 27.29
date: 1995/04/20 01:47:37; author: tbr; state: Exp; lines: +4 -2
change default recipient of pages to current user for gards
=====

RCS file: /s6/cvsroot/eutерpe/verilog/bsrc/eutерpe.V,v
Working file: verilog/bsrc/eutерpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431; selected revisions: 7
description:
-----
revision 6.405
date: 1995/04/20 23:34:11; author: billz; state: Exp; lines: +2 -2
Had an extra comma.
-----
revision 6.404
date: 1995/04/20 23:15:49; author: billz; state: Exp; lines: +4 -1
Have added LTdirtyR12 signal. Logically equivalent to LTctPaR12[0],
used to solve timing problem by splitting into half-swing (data) and
full-swing (control) signals.

A coordinated checkin of at, cc, eutерpe.V has been made.
-----
revision 6.403
date: 1995/04/20 19:59:48; author: dickson; state: Exp; lines: +3 -3
    wire [14:4] D(AUndx1500R2);
    wire [15:2] D(AUndx1500cR2);

changed these bit fields to eliminate extra loading within au
so its standalone place and route converges. ie there were some
unused outputs of au that were causing extra internal loads.
-----
revision 6.402
date: 1995/04/19 17:31:04; author: vo; state: Exp; lines: +6 -6

```

euterpe.V : changed buft driver to fullswing version to drive ecl2cmos converter  
genpin2.pl : added placement for ubill\* and buft driver  
toplev.power.tab.local : added don't prune directives for above drivers .  
-----

revision 6.401

date: 1995/04/19 04:45:28; author: tbr; state: Exp; lines: +2 -7  
delete unnecessary bufts to temp sensor  
-----

revision 6.400

date: 1995/04/18 19:37:16; author: woody; state: Exp; lines: +2 -1  
Connected Global Access interface between CE and LT.  
passed 5woody.  
-----

revision 6.399

date: 1995/04/17 21:51:04; author: dickson; state: Exp; lines: +3 -2  
added CEga\_abm [2:0] to cerberus interface  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v

Working file: verilog/bsrc/euterpe.status

head: 24.83

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 83; selected revisions: 2

description:  
-----

revision 24.59

date: 1995/04/18 07:40:40; author: mws; state: Exp; lines: +6 -1  
Add notes on detail bit bugs & cachesize=0 tag X sensitivity.  
-----

revision 24.58

date: 1995/04/17 19:44:25; author: mws; state: Exp; lines: +58 -21  
Add notes on detail bit bugs & cachesize=0 tag X sensitivity.  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe\_wrap.V,v

Working file: verilog/bsrc/euterpe\_wrap.V

head: 15.104

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 104; selected revisions: 1

description:  
-----

revision 15.92

date: 1995/04/20 14:35:44; author: lisar; state: Exp; lines: +20 -26  
Reordered dumpvars  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/fence.srf,v

Working file: verilog/bsrc/fence.srf

head: 284.2

branch:

locks: strict



```

access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 284.1
date: 1995/04/19 17:27:55; author: vo; state: Exp;
routing for ckfroot* signals and the shield wire
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/geert_v2e.config,v
Working file: verilog/bsrc/geert_v2e.config
head: 280.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 280.1
date: 1995/04/16 22:10:59; author: tbr; state: Exp;
added this so no one else gets caught out
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/genpim2.pl,v
Working file: verilog/bsrc/genpim2.pl
head: 41.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;      selected revisions: 1
description:
-----
revision 41.15
date: 1995/04/19 17:31:08; author: vo; state: Exp; lines: +4 -3
euterpe.V : changed buft driver to fullswing version to drive ecl2cmos converter
genpim2.pl : added placement for ubill* and buft driver
toplev.power.tab.local : added don't prune directives for above drivers .
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/toplev.power.tab.local,v
Working file: verilog/bsrc/toplev.power.tab.local
head: 35.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 35.2
date: 1995/04/19 17:31:09; author: vo; state: Exp; lines: +6 -1
euterpe.V : changed buft driver to fullswing version to drive ecl2cmos converter
genpim2.pl : added placement for ubill* and buft driver
toplev.power.tab.local : added don't prune directives for above drivers .

```

```

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v
Working file: verilog/bsrc/at/BOM
head: 93.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 184;   selected revisions: 2
description:
releasebom adding BOM
-----
revision 70.0
date: 1995/04/17 09:26:04; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/at

```

```

cc/at/sr location change
-----

```

```

revision 69.1
date: 1995/04/17 09:25:58; author: dickson; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/Makefile,v
Working file: verilog/bsrc/at/Makefile
head: 1.18
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 18;   selected revisions: 1
description:
-----
revision 1.17
date: 1995/04/17 09:25:04; author: dickson; state: Exp; lines: +2 -2
cc/sr/at relocation
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.V,v
Working file: verilog/bsrc/at/at.V
head: 1.66
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 66;   selected revisions: 1
description:
-----
revision 1.51
date: 1995/04/20 23:07:14; author: billz; state: Exp; lines: +4 -2
Added dirtyR11R12 output, a full swing copy of ctPaR11R12[0].
Updated placement.

```

This placement does not converge. Fails timing with at 6.3 pS over on a seemingly unrelated path, can you live with that?

I'm making a coordinated checkin of at/cc/euterpe.V .

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.pim,v  
Working file: verilog/bsrc/at/at.pim  
head: 51.23  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 23;     selected revisions: 2  
description:

-----

revision 51.10  
date: 1995/04/20 23:07:18; author: billz; state: Exp; lines: +2 -0  
Added dirtyR11R12 output, a full swing copy of ctPaR11R12[0].  
Updated placement.

This placement does not converge. Fails timing with at 6.3 pS  
over on a seemingly unrelated path, can you live with that?

I'm making a coordinated checkin of at/cc/euterpe.V .

=====

revision 51.9  
date: 1995/04/17 09:25:06; author: dickson; state: Exp; lines: +1367 -1371  
cc/sr/at relocation

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/clean-request,v  
Working file: verilog/bsrc/at/clean-request  
head: 4.11  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 11;     selected revisions: 1  
description:

-----

revision 4.8  
date: 1995/04/17 09:25:08; author: dickson; state: Exp; lines: +1 -0  
cc/sr/at relocation

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/genpim.pl,v  
Working file: verilog/bsrc/at/genpim.pl  
head: 3.12  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 12;     selected revisions: 1  
description:

-----

revision 3.12  
date: 1995/04/17 09:25:09; author: dickson; state: Exp; lines: +4 -4  
cc/sr/at relocation

=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/BOM,v
Working file: verilog/bsrc/au/BOM
head: 44.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 89;   selected revisions: 6
description:
-----
revision 38.0
date: 1995/04/20 20:01:55; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/au

fix place and route so that it converges standalone
-----
revision 37.1
date: 1995/04/20 20:01:48; author: dickson; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 37.0
date: 1995/04/18 17:22:23; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/au

timing fix for extra address bus out duplicated ffs took out buffers
-----
revision 36.1
date: 1995/04/18 17:22:16; author: dickson; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 36.0
date: 1995/04/15 21:13:30; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/au

add components for buffer copy of address output
-----
revision 35.1
date: 1995/04/15 21:13:23; author: dickson; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/au.power.tab.top,v
Working file: verilog/bsrc/au/au.power.tab.top
head: 16.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;   selected revisions: 1
description:
-----
revision 16.9
date: 1995/04/20 19:56:45; author: dickson; state: Exp; lines: +26 -0
pruned unused output gates and added power levels in au.power.tab.top
for new outputs
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/auindx.V,v
Working file: verilog/bsrc/au/auindx.V
head: 1.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 2
description:
-----
revision 1.24
date: 1995/04/20 19:56:48; author: dickson; state: Exp; lines: +3 -16
pruned unused output gates and added power levels in au.power.tab.top
for new outputs
-----
revision 1.23
date: 1995/04/18 17:20:46; author: dickson; state: Exp; lines: +17 -17
changed extra address bus out from buf_1 drivers to xorff2_1's
timing fix
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/auindx.pim,v
Working file: verilog/bsrc/au/auindx.pim
head: 12.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
-----
revision 12.9
date: 1995/04/15 21:12:24; author: dickson; state: Exp; lines: +16 -0
add components to pim file for copy of auindx address output.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/clean-request,v
Working file: verilog/bsrc/au/clean-request
head: 14.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 1
description:
-----
revision 14.7
date: 1995/04/18 17:20:48; author: dickson; state: Exp; lines: +2 -1
changed extra address bus out from buf_1 drivers to xorff2_1's
timing fix
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v
Working file: verilog/bsrc/cc/BOM
head: 92.0
branch:

```

```

locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 6
description:
releasebom adding BOM
-----
revision 80.0
date: 1995/04/19 00:41:40; author: billz; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/cc

Fixed not-mutually-exclusive state transition arcs coming
out of state M1 in ccseq. Thanks to jeffm for sleuthing
this problem. Updated placement. Looks good.
-----
revision 79.1
date: 1995/04/19 00:41:30; author: billz; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
-----
revision 79.0
date: 1995/04/18 19:40:19; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

lt, euterpe.V
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

uu:
Added an additional copy of rDstR2 and vldUW to reduce loading.
Updated placement. Added in some alignment marks.
from gards/uu-final:
    BJT Totals:      3822    27964    59585    45822    38774    18436
20 paths still fail timing.

passed 5woody.
-----
revision 78.1
date: 1995/04/18 19:40:11; author: woody; state: Exp; lines: +6 -5
releasebom: File needs to be up-to-date to use commit -r
-----
revision 78.0
date: 1995/04/17 09:31:11; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/cc

cc/at/sr loacation change
-----
revision 77.1
date: 1995/04/17 09:31:04; author: dickson; state: Exp; lines: +10 -8
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/Makefile,v
Working file: verilog/bsrc/cc/Makefile
head: 1.27
branch:
locks: strict
access list:

```

```

keyword substitution: kv
total revisions: 27;    selected revisions: 3
description:
-----
revision 1.27
date: 1995/04/20 23:10:10;  author: billz;  state: Exp;  lines: +2 -2
Two changes to fix timing.
1) dirtyR11R12 full swing input added.  This splits un net length and loads
and allows half swing signal to be used.
2) output of hexcount is replicated so that full-swing signals can be
fed-back, half-swing signals can travel some distance.

```

I'm making a coordinated checkin of at, cc and euterpe.V.

```

-----
revision 1.26
date: 1995/04/18 17:49:48;  author: billz;  state: Exp;  lines: +2 -4
Improved placement to control collisions.
Here, control_blob gets its own origin. cc_pbb is included
as a flat pim file.
-----
revision 1.25
date: 1995/04/17 09:30:22;  author: dickson;  state: Exp;  lines: +3 -1
moved billz's layout to left need more room for at
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
Working file: verilog/bsrc/cc/cc.V
head: 1.87
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 87;    selected revisions: 1
description:
-----

```

```

revision 1.80
date: 1995/04/20 23:10:13;  author: billz;  state: Exp;  lines: +8 -7
Two changes to fix timing.
1) dirtyR11R12 full swing input added.  This splits un net length and loads
and allows half swing signal to be used.
2) output of hexcount is replicated so that full-swing signals can be
fed-back, half-swing signals can travel some distance.

```

I'm making a coordinated checkin of at, cc and euterpe.V.

```

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc_control_blob.pim,v
Working file: verilog/bsrc/cc/cc_control_blob.pim
head: 77.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 2
description:
-----
revision 77.3

```

date: 1995/04/20 23:10:15; author: billz; state: Exp; lines: +7 -5  
Two changes to fix timing.  
1) dirtyR11R12 full swing input added. This splits un net length and loads  
and allows half swing signal to be used.  
2) output of hexcount is replicated so that full-swing signals can be  
fed-back, half-swing signals can travel some distance.

I'm making a coordinated checkin of at, cc and euterpe.V.

-----  
revision 77.2  
date: 1995/04/19 00:40:16; author: billz; state: Exp; lines: +3 -1  
Fixed not-mutually-exclusive state transition arcs coming  
out of state M1 in ccseq. Thanks to jeffm for sleuthing  
this problem. Updated placement. Looks good.  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc\_misc.pim,v  
Working file: verilog/bsrc/cc/cc\_misc.pim  
head: 73.3  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 3; selected revisions: 1  
description:  
-----

revision 73.3  
date: 1995/04/18 17:49:50; author: billz; state: Exp; lines: +5 -5  
Improved placement to control collisions.  
Here, control\_blob gets its own origin. cc\_pbb is included  
as a flat pim file.  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc\_pbb.pim,v  
Working file: verilog/bsrc/cc/cc\_pbb.pim  
head: 78.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1; selected revisions: 1  
description:  
-----

revision 78.1  
date: 1995/04/18 17:49:52; author: billz; state: Exp;  
Improved placement to control collisions.  
Here, control\_blob gets its own origin. cc\_pbb is included  
as a flat pim file.  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccfillcount.pla,v  
Working file: verilog/bsrc/cc/ccfillcount.pla  
head: 80.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv



total revisions: 1;      selected revisions: 1  
description:

-----  
revision 80.1

date: 1995/04/20 23:10:17;    author: billz;    state: Exp;  
Two changes to fix timing.

1) dirtyR11R12 full swing input added. This splits un net length and loads  
and allows half swing signal to be used.  
2) output of hexcount is replicated so that full-swing signals can be  
fed-back, half-swing signals can travel some distance.

I'm making a coordinated checkin of at, cc and euterpe.V.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cchexcount.pla,v

Working file: verilog/bsrc/cc/cchexcount.pla

head: 28.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 6;      selected revisions: 1

description:

-----  
revision 28.6

date: 1995/04/20 23:10:19;    author: billz;    state: Exp;    lines: +10 -8  
Two changes to fix timing.

1) dirtyR11R12 full swing input added. This splits un net length and loads  
and allows half swing signal to be used.  
2) output of hexcount is replicated so that full-swing signals can be  
fed-back, half-swing signals can travel some distance.

I'm making a coordinated checkin of at, cc and euterpe.V.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccseq.Veqn,v

Working file: verilog/bsrc/cc/ccseq.Veqn

head: 28.20

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 20;      selected revisions: 1

description:

-----  
revision 28.20

date: 1995/04/19 00:40:19;    author: billz;    state: Exp;    lines: +2 -2  
Fixed not-mutually-exclusive state transition arcs coming  
out of state M1 in ccseq. Thanks to jeffm for sleuthing  
this problem. Updated placement. Looks good.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/clean-request,v

Working file: verilog/bsrc/cc/clean-request

head: 14.13

branch:

locks: strict

```

access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
-----
revision 14.12
date: 1995/04/17 09:30:23; author: dickson; state: Exp; lines: +1 -0
moved billz's layout to left need more room for at
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/genpim.pl,v
Working file: verilog/bsrc/cc/genpim.pl
head: 5.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 3
description:
-----
revision 5.19
date: 1995/04/19 00:40:21; author: billz; state: Exp; lines: +1 -6
Fixed not-mutually-exclusive state transition arcs coming
out of state M1 in ccseq. Thanks to jeffm for sleuthing
this problem. Updated placement. Looks good.
-----
revision 5.18
date: 1995/04/18 17:49:53; author: billz; state: Exp; lines: +12 -5
Improved placement to control collisions.
Here, control_blob gets its own origin. cc_pbb is included
as a flat pim file.
-----
revision 5.17
date: 1995/04/17 09:30:25; author: dickson; state: Exp; lines: +2 -3
moved billz's layout to left need more room for at
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/pimlib.pl,v
Working file: verilog/bsrc/cc/pimlib.pl
head: 5.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
-----
revision 5.16
date: 1995/04/18 17:49:55; author: billz; state: Exp; lines: +3 -8
Improved placement to control collisions.
Here, control_blob gets its own origin. cc_pbb is included
as a flat pim file.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/BOM,v
Working file: verilog/bsrc/cdio/BOM
head: 55.0

```

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 110;   selected revisions: 4
description:
releasebom adding BOM
-----
revision 49.0
date: 1995/04/20 20:46:21;  author: tbr;   state: Exp;   lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

2nd try after a problem with a stale entry in my cdio/CVS/Entries file.

Tim

```

-----
revision 48.1
date: 1995/04/20 20:46:14;  author: tbr;   state: Exp;   lines: +1 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 48.0
date: 1995/04/19 00:48:11;  author: billz;  state: Exp;   lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

A new cc/ccseq just might fix cachenasty3.  
Placement is updated.

```

-----
revision 47.1
date: 1995/04/19 00:48:01;  author: billz;  state: Exp;   lines: +2 -1
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v
Working file: verilog/bsrc/ce/BOM
head: 86.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 170;   selected revisions: 6
description:
releasebom adding BOM
-----

```

```

revision 77.0
date: 1995/04/20 20:37:41;  author: tbr;   state: Exp;   lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

Cerberus changes to octlet 6/7 for gva and hermes machine checks

Several nit fixes to .checkoutrc's

added kludge ikos version of cg/cgclockbias

Latest Makefiles including PLL fence wires

```

genpim2.pl places oddbal top level cells
-----
revision 76.1
date: 1995/04/20 20:37:34; author: tbr; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
-----
revision 76.0
date: 1995/04/19 04:49:53; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Pick up all latest cerberus fixes.
Remove unneeded buft's from top level
-----
revision 75.1
date: 1995/04/19 04:49:46; author: tbr; state: Exp; lines: +7 -7
releasebom: File needs to be up-to-date to use commit -r
-----
revision 75.0
date: 1995/04/18 19:40:48; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

lt, euterpe.V
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

uu:
Added an additional copy of rDstR2 and vldUW to reduce loading.
Updated placement. Added in some alignment marks.
from gards/uu-final:
      BUT Totals:      3822      27964      59585      45822      38774      18436
20 paths still fail timing.

passed 5woody.
-----
revision 74.1
date: 1995/04/18 19:40:41; author: woody; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/Makefile.gards,v
Working file: verilog/bsrc/ce/Makefile.gards
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;      selected revisions: 2
description:
-----
revision 1.13
date: 1995/04/19 23:03:37; author: vo; state: Exp; lines: +1 -2
hunt-nits edits
-----
revision 1.12
date: 1995/04/19 00:57:03; author: vo; state: Exp; lines: +20 -20
Makefile.gards : got rid of rsh .

```

```

*.V : Added buffer for top level signal
cerberus.cpfif : updated to match all changes todate .
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_cms2ecl.V,v
Working file: verilog/bsrc/ce/ce_cms2ecl.V
head: 2.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 1
description:
-----
revision 2.16
date: 1995/04/19 00:57:06; author: vo; state: Exp; lines: +3 -3
Makefile.gards : got rid of rsh .
*.V : Added buffer for top level signal
cerberus.cpfif : updated to match all changes todate .
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_mck.V,v
Working file: verilog/bsrc/ce/ce_mck.V
head: 32.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
-----
revision 32.9
date: 1995/04/19 00:57:09; author: vo; state: Exp; lines: +4 -1
Makefile.gards : got rid of rsh .
*.V : Added buffer for top level signal
cerberus.cpfif : updated to match all changes todate .
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cecore.V,v
Working file: verilog/bsrc/ce/cecore.V
head: 1.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 1
description:
-----
revision 1.21
date: 1995/04/19 00:57:12; author: vo; state: Exp; lines: +24 -12
Makefile.gards : got rid of rsh .
*.V : Added buffer for top level signal
cerberus.cpfif : updated to match all changes todate .
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.V,v
Working file: verilog/bsrc/ce/cerberus.V

```

...

```

head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63;    selected revisions: 1
description:
-----
revision 1.51
date: 1995/04/17 21:48:31; author: dickson; state: Exp; lines: +4 -3
    3) standardize selftest and interrupt. interrupt at 54.

    The 3 bit field is to be located in Cerberus register 6,
    with some existing fields resized and moved within
    the register.

    old layout:      31 30 29 28 27 26 25 24 23 22 21 20
                     0  mm  -----i$-----  -----d$-----

    new layout:      31 30 29 28 27 26 25 24 23 22 21 20
                     mm  ---ga---  -----i$-----  -----d$-----

    The mm (memory management enable) bit moves from 30 to 31,
    and the i$ and d$ size fields are reduced to 4 bits each,
    making room for the 3-bit global-access field.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.cpf,v
Working file: verilog/bsrc/ce/cerberus.cpf
head: 1.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 2
description:
-----
revision 1.25
date: 1995/04/20 20:31:16; author: vo; state: Exp; lines: +2 -0
added placemnt for sc06,sc07
-----
revision 1.24
date: 1995/04/19 00:57:42; author: vo; state: Exp; lines: +1837 -1803
Makefile.gards : got rid of rsh .
*.V : Added buffer for top level signal
cerberus.cpf : updated to match all changes todate .
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbtest.V,v
Working file: verilog/bsrc/ce/cerbtest.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1

```

description:

-----  
revision 1.39

date: 1995/04/17 21:48:33; author: dickson; state: Exp; lines: +3 -2  
3) standardize selftest and interrupt. interrupt at 54.

The 3 bit field is to be located in Cerberus register 6,  
with some existing fields resized and moved within  
the register.

old layout:	31	30	29	28	27	26	25	24	23	22	21	20
	0	mm	-----i\$-----				-----d\$-----					

new layout:	31	30	29	28	27	26	25	24	23	22	21	20
	mm	---ga---		-----i\$-----				-----d\$-----				

The mm (memory management enable) bit moves from 30 to 31,  
and the i\$ and d\$ size fields are reduced to 4 bits each,  
making room for the 3-bit global-access field.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ceregcore.V,v

Working file: verilog/bsrc/ce/ceregcore.V

head: 1.44

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 44; selected revisions: 4

description:

-----  
revision 1.38

date: 1995/04/20 18:53:19; author: dickson; state: Exp; lines: +2 -2  
default ga\_abm = 100

-----  
revision 1.37

date: 1995/04/20 18:45:26; author: dickson; state: Exp; lines: +7 -2  
hooked up machine check detail bits.

-----  
revision 1.36

date: 1995/04/19 00:57:58; author: vo; state: Exp; lines: +21 -9  
Makefile.gards : got rid of rsh .

\*.V : Added buffer for top level signal  
cerberus.cpfif : updated to match all changes todate .

-----  
revision 1.35

date: 1995/04/17 21:48:35; author: dickson; state: Exp; lines: +19 -18  
3) standardize selftest and interrupt. interrupt at 54.

The 3 bit field is to be located in Cerberus register 6,  
with some existing fields resized and moved within  
the register.

old layout:	31	30	29	28	27	26	25	24	23	22	21	20
	0	mm	-----i\$-----				-----d\$-----					

```

new layout:      31 30 29 28 27 26 25 24 23 22 21 20
                mm  ---ga---  -----i$-----  -----d$-----

```

The mm (memory management enable) bit moves from 30 to 31,  
and the i\$ and d\$ size fields are reduced to 4 bits each,  
making room for the 3-bit global-access field.

=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cg/BOM,v

```

```

Working file: verilog/bsrc/cg/BOM

```

```

head: 11.0

```

```

branch:

```

```

locks: strict

```

```

access list:

```

```

keyword substitution: kv

```

```

total revisions: 20;      selected revisions: 2

```

```

description:

```

```

releasebom adding BOM

```

```

-----
revision 10.0

```

```

date: 1995/04/20 20:38:02; author: tbr; state: Exp; lines: +1 -1

```

```

Release Target: euterpe/verilog/bsrc

```

Cerberus changes to octlet 6/7 for gva and hermes machine checks

Several nit fixes to .checkoutrc's

added kludge ikos version of cg/cgclockbias

Latest Makefiles including PLL fence wires

genpin2.pl places oddbal top level cells

```

-----
revision 9.1

```

```

date: 1995/04/20 20:37:56; author: tbr; state: Exp; lines: +2 -1

```

```

releasebom: File needs to be up-to-date to use commit -r

```

=====

```

RCS file:

```

```

/s6/cvsroot/euterpe/verilog/bsrc/cg/cgclockbias.v.for_use_with_squelsh_buffer,v

```

```

Working file: verilog/bsrc/cg/cgclockbias.v.for_use_with_squelsh_buffer

```

```

head: 9.1

```

```

branch:

```

```

locks: strict

```

```

access list:

```

```

keyword substitution: kv

```

```

total revisions: 1;      selected revisions: 1

```

```

description:

```

```

-----
revision 9.1

```

```

date: 1995/04/20 13:59:15; author: lisar; state: Exp;

```

This is a hacked derived file. It comments out the buffers that short  
all of the clocks together. It is necessary in IKOS simulation to use this  
file.

Of course if the baseplate changes, it will need to change too - by hand.



```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/.checkoutrc,v
Working file: verilog/bsrc/ctiod/.checkoutrc
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 1
description:
-----
```

```
revision 1.3
date: 1995/04/19 23:37:48; author: brianl; state: Exp; lines: +2 -2
Replace clio reference with hard038
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/BOM,v
Working file: verilog/bsrc/ctiod/BOM
head: 31.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 61;      selected revisions: 2
description:
releasebom adding BOM
-----
```

```
revision 26.0
date: 1995/04/20 20:38:42; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

Cerberus changes to octlet 6/7 for gva and hermes machine checks

Several nit fixes to .checkoutrc's

added kludge ikos version of cg/cgclockbias

Latest Makefiles including PLL fence wires

genpim2.pl places oddbal top level cells

```
-----
revision 25.1
date: 1995/04/19 23:38:18; author: brianl; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctiod
               .checkoutrc
```

Replace clio reference with hard038

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/.checkoutrc,v
Working file: verilog/bsrc/dr/.checkoutrc
head: 32.6
branch:
locks: strict
access list:
```

```

keyword substitution: kv
total revisions: 6;      selected revisions: 1
description:
-----
revision 32.4
date: 1995/04/19 23:39:52; author: brianl; state: Exp; lines: +2 -2
Replace clio reference with hard038
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/BOM,v
Working file: verilog/bsrc/dr/BOM
head: 77.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 155;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 70.0
date: 1995/04/20 20:47:59; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

2nd try after a problem with a stale entry in my cdio/CVS/Entries file.

Tim
-----
revision 69.1
date: 1995/04/19 23:40:13; author: brianl; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr
        .checkoutrc

Replace clio reference with hard038
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 194;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 84.0
date: 1995/04/17 19:33:03; author: geert; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt

Rebuild gt with new genptab file

Geetr
-----
revision 83.1

```

date: 1995/04/17 19:32:56; author: geert; state: Exp; lines: +3 -3  
releasebom: File needs to be up-to-date to use commit -r

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/clean-request,v  
Working file: verilog/bsrc/gt/clean-request

head: 41.8

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 8; selected revisions: 1

description:

-----  
revision 41.6

date: 1995/04/17 19:32:22; author: geert; state: Exp; lines: +2 -1

Build gt again, please

Geert

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/genptab.pl,v

Working file: verilog/bsrc/gt/genptab.pl

head: 24.8

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 8; selected revisions: 1

description:

-----  
revision 24.5

date: 1995/04/17 19:31:31; author: geert; state: Exp; lines: +1 -6

Took out power-settings for UgvaR8R8a & b (path to LT)

Geert

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/.checkoutrc,v

Working file: verilog/bsrc/hc/.checkoutrc

head: 35.10

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 10; selected revisions: 1

description:

-----  
revision 35.9

date: 1995/04/19 23:41:24; author: brianl; state: Exp; lines: +3 -3

Replace clcio reference with hard038

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v

Working file: verilog/bsrc/hc/BOM

head: 125.0

branch:

```

locks: strict
access list:
keyword substitution: kv
total revisions: 250;   selected revisions: 5
description:
releasebom adding BOM
-----
revision 104.0
date: 1995/04/20 05:44:16; author: billz; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

Updated placement to fix NBhclprbgrant timing path
and cells flopping over clock spar on rhs.
-----
revision 103.2
date: 1995/04/20 05:44:10; author: billz; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 103.1
date: 1995/04/19 23:41:44; author: brianl; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc
        .checkoutrc

Replace clio reference with hard038
-----
revision 103.0
date: 1995/04/18 19:43:07; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

lt, euterpe.V
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

uu:
Added an additional copy of rDstR2 and vldUW to reduce loading.
Updated placement. Added in some alignment marks.
from gards/uu-final:
      BJT Totals:      3822      27964      59585      45822      38774      18436
20 paths still fail timing.

passed 5woody.
-----
revision 102.1
date: 1995/04/18 19:43:00; author: woody; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc1.power.tab.top,v
Working file: verilog/bsrc/hc/hc1.power.tab.top
head: 68.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;   selected revisions: 1
description:
-----

```

revision 63.7  
date: 1995/04/18 04:50:27; author: tbr; state: Exp; lines: +318 -324  
latest power level from top level

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc1\_control.pim,v  
Working file: verilog/bsrc/hc/hc1\_control.pim  
head: 73.15  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 15; selected revisions: 1  
description:

---

revision 73.11  
date: 1995/04/20 04:37:16; author: billz; state: Exp; lines: +1500 -2063  
Modified placement. Converges in 3 iterations, 1111 atoms.  
This placement has an additional row, row 56, on which  
the 5 cells on which NBhc1grantprb(\_N) terminate are placed.  
This should improve or eliminate NBhc1grantprb as a long  
path, \*and\* prevent cells from spilling over clock spar on  
rhs when these cells power up.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/pimlib.pl,v  
Working file: verilog/bsrc/hc/pimlib.pl  
head: 27.10  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 10; selected revisions: 1  
description:

---

revision 27.9  
date: 1995/04/20 04:37:18; author: billz; state: Exp; lines: +5 -4  
Modified placement. Converges in 3 iterations, 1111 atoms.  
This placement has an additional row, row 56, on which  
the 5 cells on which NBhc1grantprb(\_N) terminate are placed.  
This should improve or eliminate NBhc1grantprb as a long  
path, \*and\* prevent cells from spilling over clock spar on  
rhs when these cells power up.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/.checkoutrc,v  
Working file: verilog/bsrc/icc/.checkoutrc  
head: 15.4  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 4; selected revisions: 2  
description:

---

revision 15.3  
date: 1995/04/21 03:18:57; author: mws; state: Exp; lines: +2 -2

```

gards_display no longer necessary, syntax was bad anyway
=====
revision 15.2
date: 1995/04/16 02:32:37; author: mws; state: Exp; lines: +2 -2
{icc,ife}/.checkoutrc: fix guards display.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/BOM,v
Working file: verilog/bsrc/icc/BOM
head: 49.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 96; selected revisions: 4
description:
releasebom adding BOM
=====

revision 42.0
date: 1995/04/18 07:46:33; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.status: Add notes on detail bit bugs & cachesize=0 tag X sensitivity.
icc/iccxi6.Veqn icc/icc.pim.txt: Missing parentheses caused required-PL
in ITag of 2 to always cause an exception regardless of current PL.
Found by test icache_except.
ife/ife.V: Target mispredict sequential new page was treating 8K pg size
choice as 4K. Found by inspection. Placement still good.
=====

revision 41.1
date: 1995/04/18 07:46:24; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

revision 41.0
date: 1995/04/16 03:04:24; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
Try a manual placement of ife.V to replace obsolete mincut version. Since
icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix guards display.
=====

revision 40.1
date: 1995/04/16 03:04:17; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc.pim.txt,v
Working file: verilog/bsrc/icc/icc.pim.txt
head: 39.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5; selected revisions: 1
description:

```

```
-----
revision 39.2
date: 1995/04/18 07:42:01; author: mws; state: Exp; lines: +1 -1
icc/iccxc16.Veqn icc/icc.pim.txt: Missing parentheses caused required-PL
    in ITag of 2 to always cause an exception regardless of current PL.
    Found by test icache_except.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/iccxc16.Veqn,v
Working file: verilog/bsrc/icc/iccxc16.Veqn
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;    selected revisions: 1
description:
-----
```

```
revision 1.9
date: 1995/04/18 07:42:04; author: mws; state: Exp; lines: +7 -6
icc/iccxc16.Veqn icc/icc.pim.txt: Missing parentheses caused required-PL
    in ITag of 2 to always cause an exception regardless of current PL.
    Found by test icache_except.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/.checkoutrc,v
Working file: verilog/bsrc/ife/.checkoutrc
head: 18.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;    selected revisions: 2
description:
-----
```

```
revision 18.3
date: 1995/04/21 03:19:15; author: mws; state: Exp; lines: +2 -2
    gards_display no longer necessary, syntax was bad anyway
-----
```

```
revision 18.2
date: 1995/04/16 02:31:45; author: mws; state: Exp; lines: +2 -2
ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
    Try a manual placement of ife.V to replace obsolete mincut version. Since
    icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
    atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/BOM,v
Working file: verilog/bsrc/ife/BOM
head: 68.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 140;    selected revisions: 4
description:
```

```

-----
revision 63.0
date: 1995/04/18 07:47:02; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.status: Add notes on detail bit bugs & cachesize=0 tag X sensitivity.
icc/iccxc16.Veqn icc/icc.pim.txt: Missing parentheses caused required-PL
    in ITag of 2 to always cause an exception regardless of current PL.
    Found by test icache_except.
ife/ife.V: Target mispredict sequential new page was treating 8K pg size
    choice as 4K. Found by inspection. Placement still good.
-----

```

```

revision 62.1
date: 1995/04/18 07:46:52; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----

```

```

revision 62.0
date: 1995/04/16 03:04:45; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
    Try a manual placement of ife.V to replace obsolete mincut version. Since
    icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
    atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.
-----

```

```

revision 61.1
date: 1995/04/16 03:04:39; author: mws; state: Exp; lines: +7 -6
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/Makefile,v
Working file: verilog/bsrc/ife/Makefile
head: 1.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
-----

```

```

revision 1.13
date: 1995/04/16 02:31:47; author: mws; state: Exp; lines: +14 -19
ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
    Try a manual placement of ife.V to replace obsolete mincut version. Since
    icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
    atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/genpim.pl,v
Working file: verilog/bsrc/ife/genpim.pl
head: 15.7
branch:
locks: strict
access list:
keyword substitution: kv

```



```

total revisions: 7;      selected revisions: 1
description:
-----
revision 15.7
date: 1995/04/16 02:31:49; author: mws; state: Exp; lines: +15 -8
ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
    Try a manual placement of ife.V to replace obsolete mincut version. Since
    icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
    atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ife.V,v
Working file: verilog/bsrc/ife/ife.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;      selected revisions: 2
description:
-----
revision 1.44
date: 1995/04/18 07:41:13; author: mws; state: Exp; lines: +2 -2
Target mispredict sequential new page was treating 8K pg size
    choice as 4K. Found by inspection.
-----
revision 1.43
date: 1995/04/16 02:31:51; author: mws; state: Exp; lines: +7 -9
ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
    Try a manual placement of ife.V to replace obsolete mincut version. Since
    icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
    atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ife.pim.txt,v
Working file: verilog/bsrc/ife/ife.pim.txt
head: 61.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 61.1
date: 1995/04/16 02:31:53; author: mws; state: Exp;
ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
    Try a manual placement of ife.V to replace obsolete mincut version. Since
    icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
    atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/pimlib.pl,v
Working file: verilog/bsrc/ife/pimlib.pl

```

```

head: 15.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 1
description:
-----
revision 15.4
date: 1995/04/16 02:31:55; author: mws; state: Exp; lines: +10 -2
ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
    Try a manual placement of ife.V to replace obsolete mincut version. Since
    icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
    atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/BOM,v
Working file: verilog/bsrc/lt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 196;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 91.0
date: 1995/04/18 19:44:06; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

lt, euterpe.V
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

uu:
Added an additional copy of rDstr2 and vldUW to reduce loading.
Updated placement. Added in some alignment marks.
from gards/uu-final:
    BJT Totals:      3822      27964      59585      45822      38774      18436
20 paths still fail timing.

passed 5woody.
-----
revision 90.1
date: 1995/04/18 19:43:58; author: woody; state: Exp; lines: +5 -4
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/Makefile,v
Working file: verilog/bsrc/lt/Makefile
head: 3.30
branch:
locks: strict
access list:
keyword substitution: kv

```

```

total revisions: 30;    selected revisions: 1
description:
-----
revision 3.30
date: 1995/04/18 19:36:03; author: woody; state: Exp; lines: +2 -2
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

passed 5woody.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/lt.V,v
Working file: verilog/bsrc/lt/lt.V
head: 3.72
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;    selected revisions: 1
description:
-----
revision 3.72
date: 1995/04/18 19:36:06; author: woody; state: Exp; lines: +15 -5
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

passed 5woody.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/lt_control.pim,v
Working file: verilog/bsrc/lt/lt_control.pim
head: 56.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;    selected revisions: 1
description:
-----
revision 56.17
date: 1995/04/18 19:36:08; author: woody; state: Exp; lines: +13 -2
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

passed 5woody.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/ltmiss.Veqn,v
Working file: verilog/bsrc/lt/ltmiss.Veqn
head: 90.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;    selected revisions: 1
description:
-----

```

revision 90.1  
date: 1995/04/18 19:36:09; author: woody; state: Exp;  
Added the logic to support the new Global Access field in cerberus octlet 6.  
Updated placement.

passed 5woody.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/.checkoutrc,v  
Working file: verilog/bsrc/nb/.checkoutrc  
head: 46.7  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 7; selected revisions: 1  
description:

-----

revision 46.6  
date: 1995/04/19 23:43:09; author: brianl; state: Exp; lines: +2 -2  
Replace clio reference with hard038

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/BOM,v  
Working file: verilog/bsrc/nb/BOM  
head: 130.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 261; selected revisions: 2  
description:  
releasebom adding BOM

-----

revision 122.0  
date: 1995/04/20 20:50:26; author: tbr; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

2nd try after a problem with a stale entry in my cdio/CVS/Entries file.

Tim

-----

revision 121.1  
date: 1995/04/19 23:43:27; author: brianl; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/nb  
.checkoutrc

Replace clio reference with hard038

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v  
Working file: verilog/bsrc/rg/BOM  
head: 136.0  
branch:  
locks: strict  
access list:

```

keyword substitution: kv
total revisions: 297;   selected revisions: 2
description:
-----
revision 116.0
date: 1995/04/19 01:12:24;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc -- cseq fix may fix cach nasty3.
rg -- changed placement to fix overlap with au
-----
revision 115.1
date: 1995/04/19 01:12:14;  author: billz;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;   selected revisions: 1
description:
-----
revision 82.19
date: 1995/04/18 21:02:58;  author: tbr;  state: Exp;  lines: +3 -0
move upper wart to left of spar
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.power.tab.top,v
Working file: verilog/bsrc/rg/rg.power.tab.top
head: 79.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;   selected revisions: 1
description:
-----
revision 79.9
date: 1995/04/18 20:43:13;  author: tbr;  state: Exp;  lines: +1409 -1633
new top level power
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/.checkoutrc,v
Working file: verilog/bsrc/sr/.checkoutrc
head: 24.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;   selected revisions: 1
description:
-----
revision 24.6

```

date: 1995/04/19 23:45:16; author: brianl; state: Exp; lines: +2 -2  
Replace clilo reference with hard038

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/BOM,v  
Working file: verilog/bsrc/sr/BOM  
head: 75.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 148; selected revisions: 4  
description:  
releasebom adding BOM  
-----

revision 63.0  
date: 1995/04/20 20:42:23; author: tbr; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

Cerberus changes to octlet 6/7 for gva and hermes machine checks

Several nit fixes to .checkoutrc's

added kludge ikos version of cg/cgclockbias

Latest Makefiles including PLL fence wires

genpim2.pl places oddbal top level cells

-----

revision 62.1  
date: 1995/04/19 23:46:20; author: brianl; state: Exp; lines: +3 -3  
Release Target: euterpe/verilog/bsrc/sr  
.checkoutrc  
sr\_eventreg.pim

Fix nits

-----

revision 62.0  
date: 1995/04/17 09:28:37; author: dickson; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc/sr

cc/sr/at location change

-----

revision 61.1  
date: 1995/04/17 09:28:31; author: dickson; state: Exp; lines: +4 -4  
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/clean-request,v  
Working file: verilog/bsrc/sr/clean-request  
head: 26.11  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 11; selected revisions: 1

```

description:
-----
revision 26.9
date: 1995/04/17 09:27:50; author: dickson; state: Exp; lines: +2 -1
cc/at/sr location change
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/genpim.pl,v
Working file: verilog/bsrc/sr/genpim.pl
head: 16.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14; selected revisions: 1
description:
-----
revision 16.14
date: 1995/04/17 09:27:51; author: dickson; state: Exp; lines: +3 -3
cc/at/sr location change
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/sr.pim,v
Working file: verilog/bsrc/sr/sr.pim
head: 51.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 1
description:
-----
revision 51.7
date: 1995/04/17 09:27:53; author: dickson; state: Exp; lines: +1667 -1663
cc/at/sr location change
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/sr_eventreg.pim,v
Working file: verilog/bsrc/sr/sr_eventreg.pim
head: 16.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5; selected revisions: 1
description:
-----
revision 16.5
date: 1995/04/19 23:45:56; author: brianl; state: Exp; lines: +2 -1
Munged path in comment. Add Id string
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict

```

```

access list:
keyword substitution: kv
total revisions: 480;    selected revisions: 6
description:
-----
revision 186.0
date: 1995/04/20 04:16:57;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu

Minor placement modifications to pack tighter around alignment marks.
-----
revision 185.1
date: 1995/04/20 04:16:49;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 185.0
date: 1995/04/18 19:46:05;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

lt, euterpe.V
Added the logic to support the new Global Access field in cerberus octlet 6.
Updated placement.

uu:
Added an additional copy of rDstR2 and vldUW to reduce loading.
Updated placement. Added in some alignment marks.
from gards/uu-final:
      BJT Totals:      3822      27964      59585      45822      38774      18436
20 paths still fail timing.

passed 5woody.
-----
revision 184.1
date: 1995/04/18 19:45:55;  author: woody;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 184.0
date: 1995/04/17 13:49:15;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu

fix genpim to use correct obstruction mask file.
-----
revision 183.1
date: 1995/04/17 13:49:06;  author: woody;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/clean-request,v
Working file: verilog/bsrc/uu/clean-request
head: 78.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;    selected revisions: 1
description:
-----

```



revision 78.9  
date: 1995/04/17 13:47:49; author: woody; state: Exp; lines: +1 -0  
fix genpim to use correct obstruction mask file.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/genpim.pl,v  
Working file: verilog/bsrc/uu/genpim.pl  
head: 68.17  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 17; selected revisions: 1  
description:

---

revision 68.17  
date: 1995/04/17 13:47:51; author: woody; state: Exp; lines: +3 -3  
fix genpim to use correct obstruction mask file.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v  
Working file: verilog/bsrc/uu/uu.V  
head: 1.202  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 202; selected revisions: 1  
description:  
issue unit

---

revision 1.179  
date: 1995/04/18 19:33:32; author: woody; state: Exp; lines: +21 -15  
Added an additional copy of rDstr2 and vldUW to reduce loading.  
Updated placement. Added in some alignment marks.  
from gards/uu-final:  
EJT Totals: 3822 27964 59585 45822 38774 18436  
20 paths still fail timing.

passed 5woody and sswap.tst

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu\_control.pim,v  
Working file: verilog/bsrc/uu/uu\_control.pim  
head: 68.60  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 60; selected revisions: 2  
description:

---

revision 68.41  
date: 1995/04/20 04:15:06; author: woody; state: Exp; lines: +39 -16  
Minor placement modifications to pack tighter around alignment marks.

---

revision 68.40

```

date: 1995/04/18 19:33:46; author: woody; state: Exp; lines: +94 -86
Added an additional copy of rDstr2 and vldUW to reduce loading.
Updated placement. Added in some alignment marks.
from gards/uu-final:
    BJT Totals:      3822    27964    59585    45822    38774    18436
20 paths still fail timing.

```

passed 5woody and sswap.tst

```

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/BOM,v
Working file: verilog/bsrc/xlu/BOM
head: 65.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 4
description:
releasebom adding BOM

```

```

-----
revision 57.0
date: 1995/04/20 20:43:08; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

Cerberus changes to octlet 6/7 for gva and hermes machine checks

Several nit fixes to .checkoutrc's

added kludge ikos version of cg/cgclockbias

Latest Makefiles including PLL fence wires

genpim2.pl places oddbal top level cells

```

-----
revision 56.1
date: 1995/04/20 20:43:00; author: tbr; state: Exp; lines: +4 -5
releasebom: File needs to be up-to-date to use commit -r
-----
revision 56.0
date: 1995/04/16 03:06:47; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

```

ife/ife.V ife/genpim.pl ife/pimlib.pl ife/ife.pim.txt(new) ife/Makefile:
  Try a manual placement of ife.V to replace obsolete mincut version. Since
  icc is now much bigger and ife much smaller, ife gets new origin, keeps 20
  atom height, but gives up L shape.
{icc,ife}/.checkoutrc: fix gards display.

```

```

-----
revision 55.1
date: 1995/04/16 03:06:40; author: mws; state: Exp; lines: +2 -1
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/x123.pim,v
Working file: verilog/bsrc/xlu/x123.pim

```

```

head: 33.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;      selected revisions: 1
description:
-----
revision 33.8
date: 1995/04/19 23:03:55;  author: vo;  state: Exp;  lines: +1 -2
hunt-nits edits
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/x126.pim,v
Working file: verilog/bsrc/xlu/x126.pim
head: 40.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 40.2
date: 1995/04/19 23:03:58;  author: vo;  state: Exp;  lines: +1 -2
hunt-nits edits
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/x456.pim,v
Working file: verilog/bsrc/xlu/x456.pim
head: 33.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 33.3
date: 1995/04/19 23:04:01;  author: vo;  state: Exp;  lines: +1 -2
hunt-nits edits
=====

```